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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,744	FONTAINE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-10, and 12-27 have been considered. Claims 1, 10, and 27 have been amended as per Applicant's request. Claims 2 and 11 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 24 November 2004 and Change of Address as filed 28 December 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 5-10, 12-13, and 14-18 are rejected under 35 U.S.C. 102(e) as being taught by Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col).

5. Referring to claim 1, Col has taught a method for processing a conditional jump instruction in a pipelined instruction processor, the method comprising:

a. Generating at least one status bit based on a digital value to be stored, the at least one status bit relating to a particular condition of a conditional jump instruction and specifying if the particular condition of the conditional jump instruction is satisfied or not (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and

53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

b. Storing the digital value and the at least one status bit to a memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

c. In response to a conditional jump instruction, reading from the memory the digital value and the at least one status bit to determine if the condition of the conditional jump instructions is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

6. Referring to claim 3, Col has taught wherein the at least one status bit is read from memory at the same time as the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

7. Referring to claim 5, Col has taught wherein the at least one status bit is set high if the digital value is zero (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

8. Referring to claim 6, Col has taught wherein the at least one status bit is set high if the digital value is a positive value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

9. Referring to claim 7, Col has taught wherein the at least one status bit is set high if the digital value is negative (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55;

column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

10. Referring to claim 8, Col has taught wherein the at least one status bit is set high if the digital value is a non zero value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

11. Referring to claim 9, Col has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

12. Referring to claim 10, Col has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, one or more of the conditional jump

instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B), the improvement comprising:

a. Status bit generator for generating at least one status bit based on a digital value, the at least one status bit indicating if a predetermined condition of a conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

b. Storing means for storing the digital value and the at least one status bit to the memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

c. Conditional jump processing means, activated in response to the execution of a conditional jump instruction, the conditional jump processing means reading from the memory the digital value and the at least one status bit to determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

13. Referring to claim 12, Col has taught wherein the at least one status bit is read from the memory at the same time as the digital value is read (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

14. Referring to claim 14, Col has taught wherein the at least one status bit is set high if the digital value is zero (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14,

lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

15. Referring to claim 15, Col has taught wherein the at least one status bit is set high if the digital value is a positive value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

16. Referring to claim 16, Col has taught wherein the at least one status bit is set high if the digital value is negative (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

17. Referring to claim 17, Col has taught wherein the at least one status bit is set high if the digital value is anon zero value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27;

column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

18. Referring to claim 18, Col has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col), as applied to claims 1 and 10 above, in view of Olson et al., U.S. Patent Number 5,824,070 (herein referred to as Olson). Col has taught wherein the memory has one or more addressable locations (Col column 16, lines 48-53). Col has not taught the at least one status bit is stored at the same addressable location as the corresponding digital value. Olson has taught the at least one status bit is stored at the same

addressable location as the corresponding digital value (Olson column 1, lines 36-40). A person of ordinary skill in the art at the time the invention was made, and as recognized in Olson, would have recognized that the status bits must be associated with the correct instruction to be visible to the user (Olson column 1, lines 31-35). Therefore, a person of ordinary skill in the art at the time the invention was made would have incorporated the status bits of Olson in the device of Col in order to ensure the status bits are associated with the correct instruction.

21. Claims 19-22 and 24-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al., U.S. Patent Number 3,573,854 (herein referred to as Watson) in view of Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col).

22. Referring to claim 19, Watson has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, the improvement comprising:

a. A plurality of addressable registers, each of the addressable registers (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

b. Logic to access a current instruction (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

c. A jump look-ahead controller for generating a jump look-ahead signal, the jump look-ahead signal is a function of the identified jump condition (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to

column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

d. Tracking logic for tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses of each previous instruction to the address of the current instruction to generate a series of jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5); and

e. Conflict detection logic for generating a jump early signal using the jump look-ahead signal and the series of jump disable signals, the jump early signal initiates the conditional jump depending on the values of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

23. Watson has not taught:

a. One or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied;

b. Storing a value that includes a digital value and at least one jump status bit;

c. Wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding

jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register; and

d. Using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register.

24. Col has taught:

a. One or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

b. Storing a value that includes a digital value and at least one jump status bit (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

c. Wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding

jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

d. Using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

25. A person of ordinary skill in the art at the time the invention was made, and as recognized in Col, would have recognized that compare-and-jump operations of Col execute without undue program delays (Col column 3, lines 41-43) and decreases the number of instructions (Col column 4, lines 3-6), thereby increasing overall processor efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compare-and-jump operations of Col to increase processor efficiency.

26. Referring to claims 20 and 21, Watson has not taught

a. Wherein each jump status bit is dependent on the digital value stored in the corresponding addressable register; and

b. A bit status generator for generating the corresponding jump status bits.

27. Col has taught:

a. Wherein each jump status bit is dependent on the digital value stored in the corresponding addressable register (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

b. A bit status generator for generating the corresponding jump status bits (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

28. A person of ordinary skill in the art at the time the invention was made, and as recognized in Col, would have recognized that compare-and-jump operations of Col execute without undue program delays (Col column 3, lines 41-43) and decreases the number of instructions (Col column 4, lines 3-6), thereby increasing overall processor efficiency. Therefore, it would have

been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compare-and-jump operations of Col to increase processor efficiency.

29. Referring to claim 22, Watson has taught a prediction logic block responsive to the jump early signal for implementing a prediction algorithm to predict the conditional jump depending on the values of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

30. Referring to claim 24, Watson has taught wherein the predetermined number of instructions are sequentially piped through an execution pipeline after being piped through a pre-fetch pipeline, the execution pipeline includes a write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

31. Referring to claim 25, Watson has taught wherein the addressable register is written during the write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

32. Referring to claim 26, Watson has taught wherein the execution pipeline further includes an address generation stage, a present address stage, an output operand stage, a capture data stage, and an arithmetic operation stage, all before the write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61;

column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

33. Referring to claim 27, Watson has taught a method for determine if a condition of a conditional jump instruction is satisfied in a pipelined instruction processor, the method comprising:

a. Generating a jump look-ahead signal that is a function of the selected jump status bit read from the selected address location of the addressable memory, the identified jump status bit is accessed using the address and the jump field of the current instruction (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

b. Tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses to the address of the current instruction to generate a series of jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5); and

c. Generating a jump early signal using the jump look-ahead signal and the series jump disable signals, the jump early signal initiates a conditional jump depending on the value of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61;

column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

34. Watson has not taught:

a. Storing a digital value and one or more jump status bits that are based on the digital value in one or more of a plurality of address locations in an addressable memory; and

b. Accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected address location.

35. Col has taught:

a. Storing a digital value and one or more jump status bits that are based on the digital value in one or more of a plurality of address locations in an addressable memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

b. Accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected

address location (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

36. A person of ordinary skill in the art at the time the invention was made, and as recognized in Col, would have recognized that compare-and-jump operations of Col execute without undue program delays (Col column 3, lines 41-43) and decreases the number of instructions (Col column 4, lines 3-6), thereby increasing overall processor efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compare-and-jump operations of Col to increase processor efficiency.

37. Claim 23 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Watson in view of Col as applied to claim 19 above, and further in view of Heuring and Jordan's Computer Systems Design and Architecture ©1997 (herein referred to as Heuring). Watson in view of Col has not taught wherein the tracking logic includes a queue for sequentially storing a pre-determined number of instructions prior to sequentially piping the pre-determined number of instructions through a read stage and decode stage in a pre-fetch pipeline. Heuring has taught wherein the tracking logic includes a queue for sequentially storing a pre-determined number of instructions prior to sequentially piping the pre-determined number of instructions through a read stage and decode stage in a pre-fetch pipeline (Heuring Pages 92-95). A person of ordinary skill in the art at the time the invention was made would have recognized that pre-fetching increases

the speed and efficiency of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the pre-fetching of Heuring to increase processor speed and efficiency.

Response to Arguments

38. Applicant's arguments filed 24 November 2004 have been fully considered but they are not persuasive.

39. Applicant's argue in essence on page 11 "...in Col, the status flags are not read from memory to determine if the condition of the conditional jump instruction is satisfied". This has not been found persuasive. The status flags are read from flags register (Col column 3, lines 29-40). A register is a memory location. Please see the FOLDOC definition of register for the definition of register.

40. Applicant's argue in essence on page 11 "...nor does Col determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor". This has not been found persuasive. Col teaches in column 16, line 58 to column 17, line 6 that the condition, or test, is not submitted, which means to subject to a process or commit to judgment of other, i.e. actually executed, until the store stage of the system. The execution stage, which has the ALU (arithmetic-logic unit), does not actually do anything more with the condition test than pass it through the stage. The execution stage performs the arithmetic or compare portion of the instruction, not the condition or test, so the condition was never submitted to the stage. Please see the American Heritage Dictionary ©2000 definition of "submit".

41. Applicant's argue on page 11 in essence

> ...the status flags of Col are not read from memory at the same time as the digital value. Instead, the status flags of Col and the digital value are stored in different locations

42. This has not been found persuasive. The claim states that they are read from memory at the same time not that they must be in the same location. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., storing the flags and value at the same location) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

43. Applicant's argue in essence on page 12

> The status flags are stored in flags register 561. Thus, Col does not appear to store the status flags at the same addressable location as the corresponding digital value...

44. This has not been found persuasive. Claim 4 was rejected under 35 USC § 103(a), so it was a combination rejection. Col was not relied upon to teach "the same addressable location" limitation, the secondary reference Olsen was. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

45. Applicant's argue in essence on page 12 "...Olsen does not appear to disclose or suggest the step of reading from memory a digital value and at least one status bit to determine...pipelines instruction process." This has not been found persuasive. Claim 4 was rejected under 35 USC § 103(a), so it was a combination rejection. Olsen was not relied upon to teach these limitations, the primary reference Col was. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

46. Applicant argues in essence on pages 13-16

> ...Applicant fail to see where an instruction is shown that includes an address and a corresponding jump field, wherein the address identifies one of the addressable register and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register.

47. This has not been found persuasive. The conditional jump is based on a bit in the flags register, i.e. the status bit, which says whether the condition is true or not. The flags register is identified inherently in the conditional jump since the system must know where to find the flag bit that the condition is based upon.

48. Applicant argues in essence on pages 13-16 "Applicants also fail to see where a number of other elements...are disclosed..." This has not been found persuasive. The Examiner cannot clarify the location of elements if she does not know which elements the Applicant cannot locate and/or identify in the cited prior art. Applicant is encouraged to contact the Examiner for

clarification if they cannot locate the limitation within the cited material. Due to the nature of the art and technology, sometimes the exact same language is not used, but the elements taught operate similarly to the claim limitations.

49. Applicant argues in essence on pages 14-16 "Applicant believes that such a rejection is improper as being unclear, and respectfully requests that the Examiner specifically point out where in Watson and/or Col each and every element...is disclosed." This has not been found persuasive. The Examiner has cited what was believed to be relevant to understanding the prior art and how it read upon the claims. The Examiner cited portions from 7 out of 14 columns and 2 out of 5 figures in Watson and portions from 12 out of 24 columns and 2 out of 8 figures in Col. The columns and figures cited all show how Watson and Col function similar to the limitations in the claims and were deemed necessary for understanding this functionality, since the terminology used within the claims and the terminology used with in the prior art are not necessarily exactly the same, but the functionality of the elements are similar. The Examiner encourages Applicant to contact her if they are unclear as to how the reference reads upon the claims and/or where the limitations are located within the references.

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

51. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

52. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

53. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

54. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
3 February 2005

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